1.1A Step-Up DC/DC Converter with Integrated Soft-Start

ADPL21210

Features

- **2.1MHz Switching Frequency**
- **Low V_{CESAT} Switch: 330mV at 1.1A**
- **High Output Voltage: Up to 24V**
- **Wide Input Range: 2.7V to 12V**
- **Dedicated Soft-Start Pin**
- Uses Small Surface Mount Components
- Low Shutdown Current: <1µA
- Low Profile (1mm) ThinSOT™ Package
- Low Profile (0.75mm) 8-Lead (3mm × 2mm) Dual Flat No Lead (DFN) Package

Applications

- Digital Cameras
- White LED Power Supplies
- Cellular Phones
- Medical Diagnostic Equipment
- Local 5V or 12V Supplies
- Thin Film Transistor (TFT)-Liquid Crystal Display (LCD) Bias Supplies
- xDigital Subscriber Line (xDSL) Power Supplies

Description

The ADPL21210 switching regulators combine a 26V, 1.1A switch with a soft-start function. The ADPL21210 switches at 2.1MHz, allowing the use of even smaller components. High inrush current at start-up is eliminated using the programmable soft-start function. A single external capacitor sets the current ramp rate. A constant-frequency current mode pulse-width modulator (PWM) architecture results in low, predictable output noise that is easy to filter.

The high-voltage switch on the ADPL21210 is rated at 26V, making the devices ideal for boost converters up to 24V, as well as SEPIC and flyback designs. The ADPL21210 is available in a low-profile (1mm) 6-lead Small outline transistor (SOT)-23 package and tiny 3mm × 2mm DFN package.

***Ordering Information* appears at end of data sheet.**

Typical Application

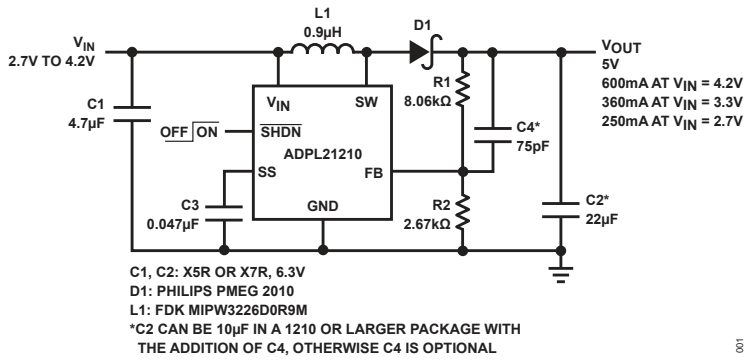

Figure 1. Single Li-Ion Cell to 5V Boost Converter

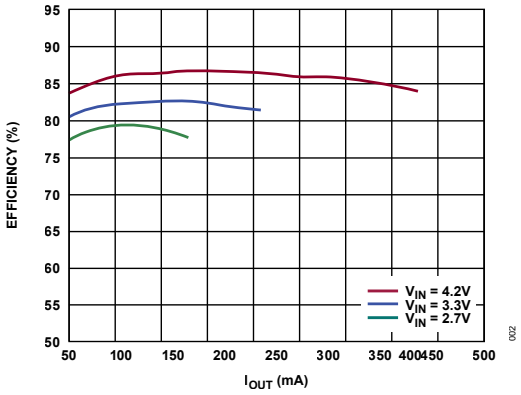

Figure 2. Efficiency vs. Load Current

Rev 0; 1/26

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Absolute Maximum Ratings (Note 1)

V_{IN} Voltage 12V
SW Voltage ..... –0.4V to 26V
FB Voltage 2.5V
Current Into FB Pin ..... ±1mA
$\overline{SHDN}$ Voltage 16V
Maximum Junction Temperature ..... 125°C

Operating Junction Temperature Range (Note 2)
E-Grade ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TSOT ..... 300°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
Note 2: The ADPL21210 are guaranteed to meet performance specifications from 0°C to 85°C, junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage				2.4	2.7	V
Maximum Operating Voltage					12	V
Feedback Voltage			1.230		1.270	V
		●	1.220	1.255	1.280	V
FB Pin Bias Current	(Note 1)	●		10	50	nA
Quiescent Current	$V_{\overline{SHDN}}$ = 2.4V, Not Switching			1.5	2	mA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0.5V, V_{IN} = 3V			0.01	1	µA
Reference Line Regulation	2.7V ≤ V_{IN} ≤ 16V			0.01	0.05	%/V
Switching Frequency			1.6	2.1	2.7	MHz
		●	1.6			MHz
Maximum Duty Cycle			82	88		%
		●	78			%
Minimum Duty Cycle				10		%
Switch Current Limit	At Minimum Duty Cycle		1.4	1.8	2	A
	At Maximum Duty Cycle (Note 2)		0.8	1.2	1.9	A
Switch V_{CESAT}	I_{SW} = 1.1A			330	500	mV
Switch Leakage Current	V_{SW} = 5V			0.01	1	µA
$\overline{SHDN}$ Input Voltage High			2.7			V
$\overline{SHDN}$ Input Voltage Low					0.5	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V			16	32	µA
	$V_{\overline{SHDN}}$ = 0V			0	0.1	µA
SS Charging Current	V_{SS} = 0.5V		2	3	4.5	µA

Note 1: Current flows out of the pin.
Note 2: See Figure 6 in Typical Performance Characteristics section for guaranteed Current Limit vs. Duty Cycle.

Typical Performance Characteristics

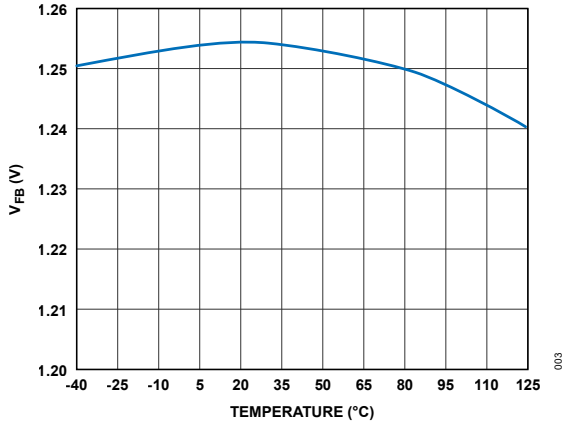


Figure 3. FB Pin Voltage vs. Temperature

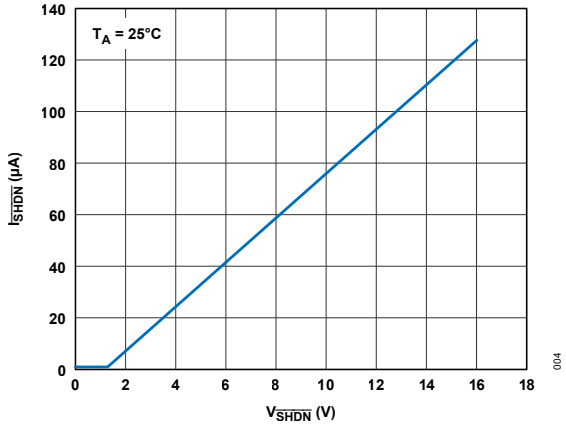


Figure 4. $\overline{SHDN}$ Current vs. $\overline{SHDN}$ Voltage

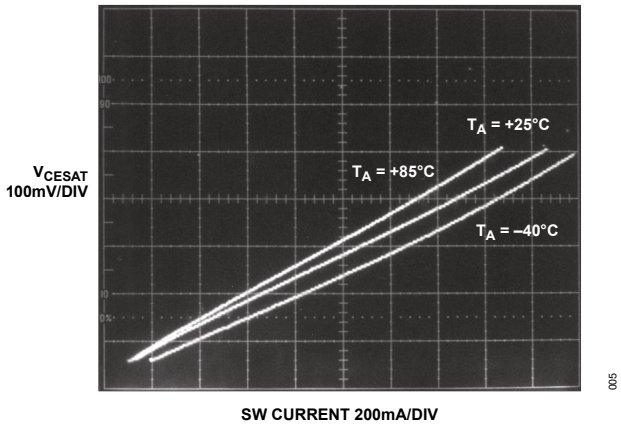


Figure 5. Switch Saturation Voltage vs. Switch Current

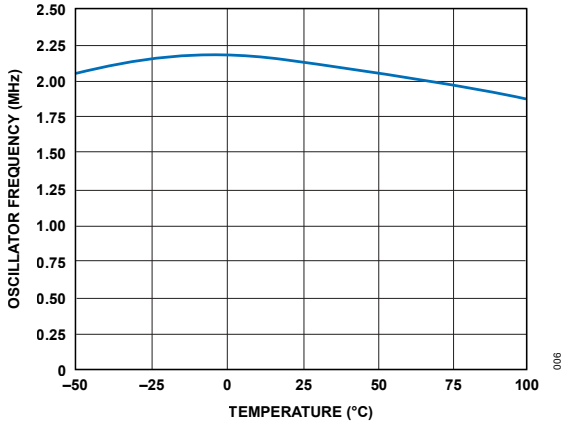


Figure 6. Oscillator Frequency vs. Temperature

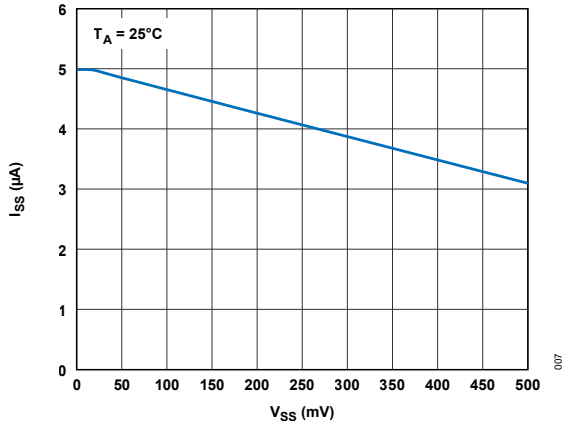


Figure 7. Soft-Start Current vs. Soft-Start Voltage

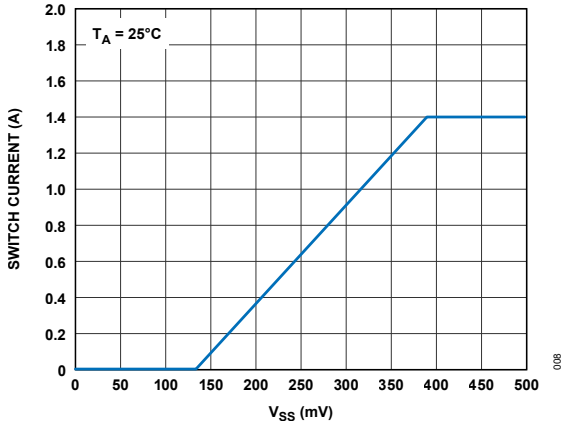


Figure 8. Peak Switch Current vs. Soft-Start Voltage

Pin Configurations

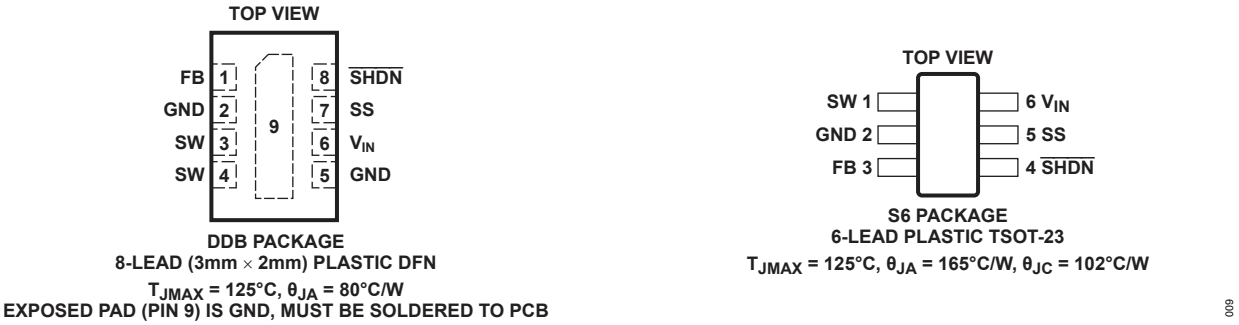


Figure 9. Pin Configurations

Pin Description

PIN		NAME	FUNCTION
DFN	TSOT		
1	3	FB	Feedback Pin. Reference voltage is 1.255V. Connect the resistive divider tap here. Minimize the trace area at FB. Set V_{OUT} = 1.255V(1 + R1/R2).
2, 5, 9	2	GND	Ground. Tie directly to the local ground plane.
3, 4	1	SW	Switch Pin. (Collector of internal Negative-positive-negative (NPN) power switch). Connect the inductor/diode here and minimize the metal trace area connected to this pin to minimize Electromagnetic interference (EMI).
6	6	V_{IN}	Input Supply Pin. Must be locally bypassed.
7	5	SS	Soft-Start Pin. Place a soft-start capacitor here. Upon start-up, 4µA of current charges the capacitor to 1.255V. Use a larger capacitor for a slower start-up. Leave floating if not in use.
8	4	$\overline{SHDN}$	Shutdown Pin. Tie to 2.4V or more to enable the device. Ground to shut down.

Block Diagram

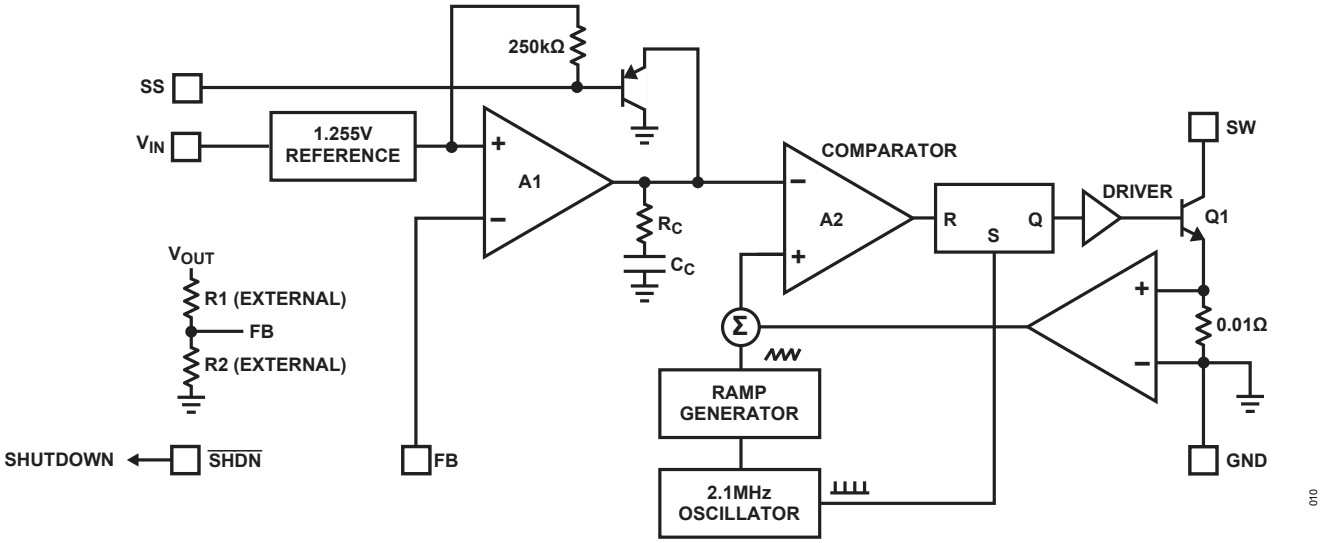


Figure 10. Block Diagram

Operation

The ADPL21210 uses a constant-frequency, current-mode control scheme to provide excellent line and load regulation. See the Block Diagram for more details. At the start of each oscillator cycle, the SR latch is set, which turns on the power switch Q1. A voltage proportional to the switch current is added to a stabilizing ramp, and the resulting sum is fed into the positive terminal of the PWM comparator A2. When this voltage exceeds the level at the negative input of A2, the SR latch is reset, turning off the power switch. The level at the negative input of A2 is set by the error amplifier A1, and is simply an amplified version of the difference between the feedback voltage and the reference voltage of 1.255V. In this manner, the error amplifier sets the correct peak current level to keep the output in regulation. If the error amplifier's output increases, more current is delivered to the output. Similarly, if the error decreases, less current is delivered. The soft-start feature of the ADPL21210 enables clean start-up conditions by limiting the rate of voltage rise at the output of comparator A1, which, in turn, limits the peak switch current. The soft-start pin is connected to a reference voltage of 1.255V through a 250kΩ resistor, providing 4µA of current to charge the soft-start capacitor. Typical values for the soft-start capacitor range from 10nF to 200nF. The ADPL21210 has a current limit circuit not shown in the Block Diagram. The switch current is constantly monitored and not allowed to exceed the maximum switch current (typically 1.4A). If the switch current reaches this value, the SR latch is reset regardless of the state of comparator A2. This current limit protects both the power switch and the external components connected to the ADPL21210.

Operation

Duty Cycle

The typical maximum duty cycle of the ADPL21210 is 88%. The duty cycle for a given application is given by:

$$DC = \frac{|V_{OUT}| + |V_D| - |V_{IN}|}{|V_{OUT}| + |V_D| - |V_{CESAT}|}$$

where V_D is the diode forward voltage drop and V_{CESAT} is, in the worst case, 330mV (at 1.1A).

The ADPL21210 can be used at higher duty cycles, but must be operated in the discontinuous conduction mode so that the actual duty cycle is reduced.

Setting Output Voltage

R1 and R2 determine the output voltage.

$$V_{OUT} = 1.255V\ (1+ R1/R2)$$

Switching Frequency and Inductor Selection

The ADPL21210 switches at 2.1MHz, allowing for even smaller valued inductors to be used. 0.9µH to 6.8µH will usually suffice. Choose an inductor that can handle at least 1.2A without saturating, and ensure that the inductor has a low DCR (copper-wire resistance) to minimize I^2R power losses. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology, where each inductor only carries one-half of the total switch current. For better efficiency, use similar valued inductors with a larger volume. Many different sizes and shapes are available from various manufacturers. Choose a core material that has low losses at 2.1MHz, such as a ferrite core.

Soft-Start

The soft-start feature provides a way to limit the inrush current drawn from the supply upon start-up. An internal 250k resistor charges the external soft-start capacitor to 1.255V. After the capacitor reaches 0.15V, the rate of voltage rise at the output of the comparator A1 tracks the rate of voltage rise of the soft-start capacitor. This limits the inrush current drawn from the supply during start-up. The soft-start feature plays another important role in applications where the switch will reach levels of 30V or higher. During start-up, excessively high switch current, together with the presence of high voltage, can overstress the switch. A properly used soft-start feature will keep the switch current from overshooting. This practice will greatly improve the robustness of such designs. Once the part is shut down, the soft-start capacitor is quickly discharged to 0.4V, then slowly discharged through the 250kΩ resistor to ground. If the part is to be shut down and re-enabled within a short period of time while using soft-start, you must ensure that the soft-start capacitor has sufficient time to discharge before re-enabling the part. Typical values of the soft-start capacitor range from 10nF to 200nF.

Capacitor Selection

Low Equivalent series resistance (ESR) capacitors should be used at the output to minimize the output ripple voltage. Multi-layer ceramic capacitors are an excellent choice, as they have extremely low ESR and are available in very small packages. X5R dielectrics are preferred, followed by X7R, as these materials retain their capacitance over a wide range of voltages and temperatures. A 4.7µF to 15µF output capacitor is sufficient for most applications; however, systems with very low output currents may require only a 1µF or 2.2µF output capacitor. Solid tantalum or OS-CON capacitors can be used, but they will occupy more board area than ceramic capacitors and will have a higher ESR. Always use a capacitor with a sufficient voltage rating.

Ceramic capacitors also make a good choice for the input decoupling capacitor, which should be placed as close as possible to the ADPL21210. A 1µF to 4.7µF input capacitor is sufficient for most applications. Table 2 lists several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 1. Inductor Manufacturers

MANUFACTURER	WEB
Sumida	www.sumida.com
TDK	www.tdk.com
Murata	www.murata.com
FDK	www.fdk.co.jp

Table 2. Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
Taiyo Yuden	www.t-yuden.com
AVX	www.avxcorp.com
Murata	www.murata.com

The decision to use either low ESR (ceramic) capacitors or the higher ESR (tantalum or OS-CON) capacitors can affect the stability of the overall system. The ESR of any capacitor, along with the capacitance itself, contributes a zero to the system. For the tantalum and OS-CON capacitors, this zero is located at a lower frequency due to the higher value of the ESR, while the zero of a ceramic capacitor is at a much higher frequency and can generally be ignored.

A phase lead zero can be intentionally introduced by placing a capacitor (C4) in parallel with the resistor (R1) between V_{OUT} and V_{FB} as shown in Figure 1. The frequency of the zero is determined by the following equation.

$$f_Z = \frac{1}{2\pi \times R1 \times C4}$$

By choosing the appropriate values for the resistor and capacitor, the zero frequency can be designed to improve the phase margin of the overall converter. The typical target value for the zero frequency is between 35kHz to 55kHz.

Diode Selection

A Schottky diode is recommended for use with the ADPL21210. The Philips PMEG 2005 is a very good choice. Where the switch voltage exceeds 20V, use the PMEG 3005 (a 30V diode). These diodes are rated to handle an average forward current of 0.5A. In applications where the average forward current of the diode exceeds 0.5A, a Philips PMEG 2010 rated at 1A is recommended. For higher efficiency, use a diode with better thermal characteristics such as the On Semiconductor MBRM120 (a 20V diode) or the MBRM140 (a 40V diode).

Setting Output Voltage

To set the output voltage, select the values of R1 and R2 (see Figure 1) according to the following equation.

$$R1 = R2 \left(\frac{V_{OUT}}{1.255V} - 1 \right)$$

A good value for R2 is 13.3kΩ which sets the current in the resistor divider chain to 1.255V/13.3kΩ = 94µA.

Layout Hints

The high speed operation of the ADPL21210 demands careful attention to board layout. You will not get advertised performance with careless layout. Figure 11a shows the recommended component placement for the ThinSOT package. Figure 11b shows the recommended component placement for the DFN package. Note the vias under the Exposed Pad. These should connect to a local ground plane for better thermal performance.

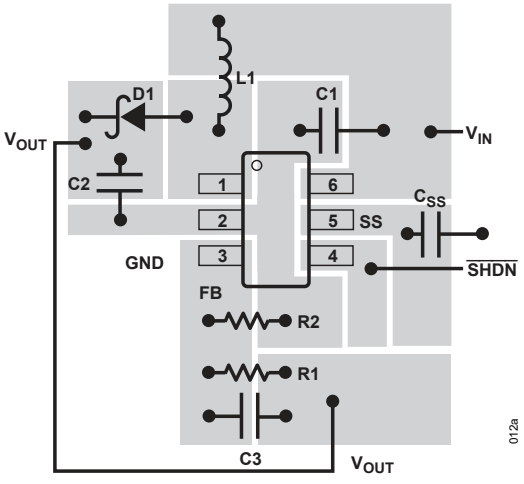


Figure 11a. Suggested Layout—ThinSOT

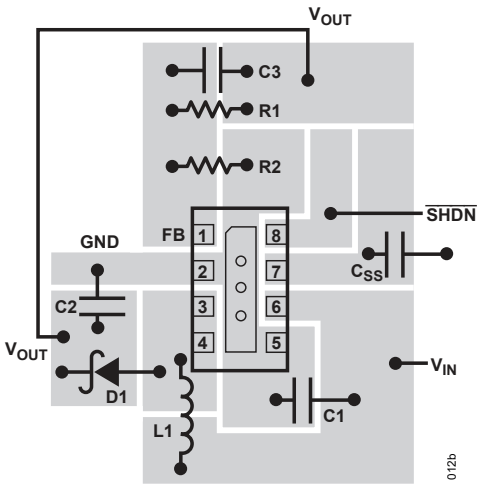


Figure 11b. Suggested Layout—DFN

Compensation—Theory

Like all other current-mode switching regulators, the ADPL21210 needs to be compensated for stable and efficient operation. Two feedback loops are used in the ADPL21210: a fast current loop, which does not require compensation, and a slower voltage loop, which does. Standard Bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 12 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by the equivalent transconductance amplifier g_{mp}. g_{mp} acts as a current source where the output current is proportional to the V_C voltage. Note that the maximum output current of the g_{mp} is finite due to the current limit in the IC.

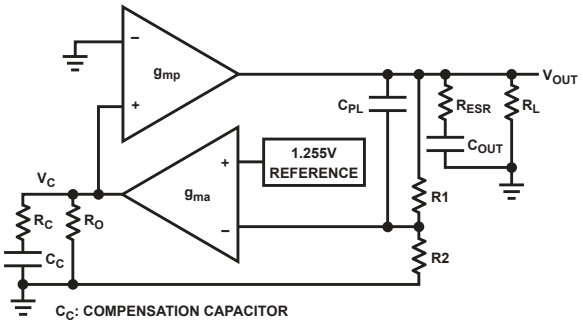


Figure 12. Boost Converter Equivalent Model

From Figure 12, the DC gain, poles and zeroes can be calculated as follows:

$$\text{Output Pole: } P1 = \frac{2}{2 \times \pi \times R_L \times C_{OUT}}$$

$$\text{Error Amp Pole: } P2 = \frac{1}{2 \times \pi \times R_0 \times C_C}$$

$$\text{Error Amp Zero: } Z1 = \frac{1}{2 \times \pi \times R_C \times C_C}$$

$$\text{DC GAIN: } A = \frac{1.255}{V_{OUT}^2} \times V_{IN} \times g_{ma} \times R_0 \times g_{mp} \times R_L \times \frac{1}{2}$$

$$\text{ESR Zero: } Z2 = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$\text{RHP Zero: } Z3 = \frac{V_{IN}^2 \times R_L}{2 \times \pi \times V_{OUT}^2 \times L}$$

$$\text{High Frequency Pole: } P3 > \frac{f_S}{3}$$

$$\text{Phase Lead Zero: } Z4 = \frac{1}{2 \times \pi \times R1 \times C_{PL}}$$

$$\text{Phase Lead Pole: } P4 = \frac{1}{2 \times \pi \times C_{PL} \times \frac{R1 \times R2}{R1 + R2}}$$

The current mode zero is a right-half plane zero, which can be an issue in feedback control design, but is manageable with proper external component selection.

Typical Application Circuit

3.3V to 15V, 135mA Stup-Up Converter

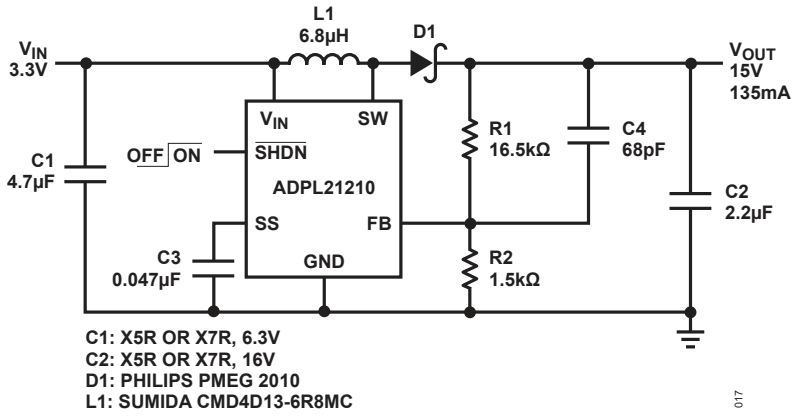
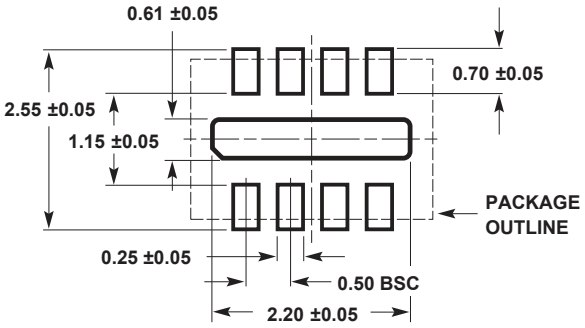


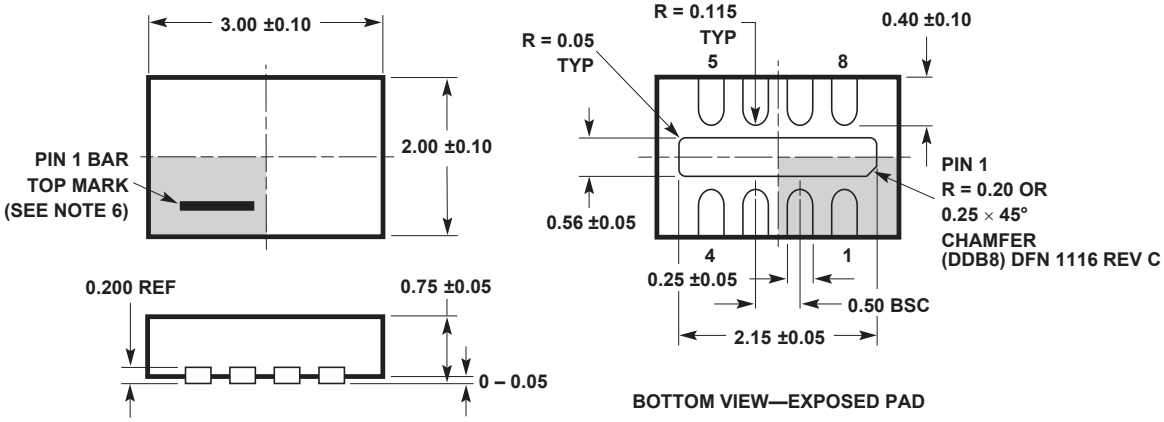
Figure 13. Typical Application Circuit

Chip Information

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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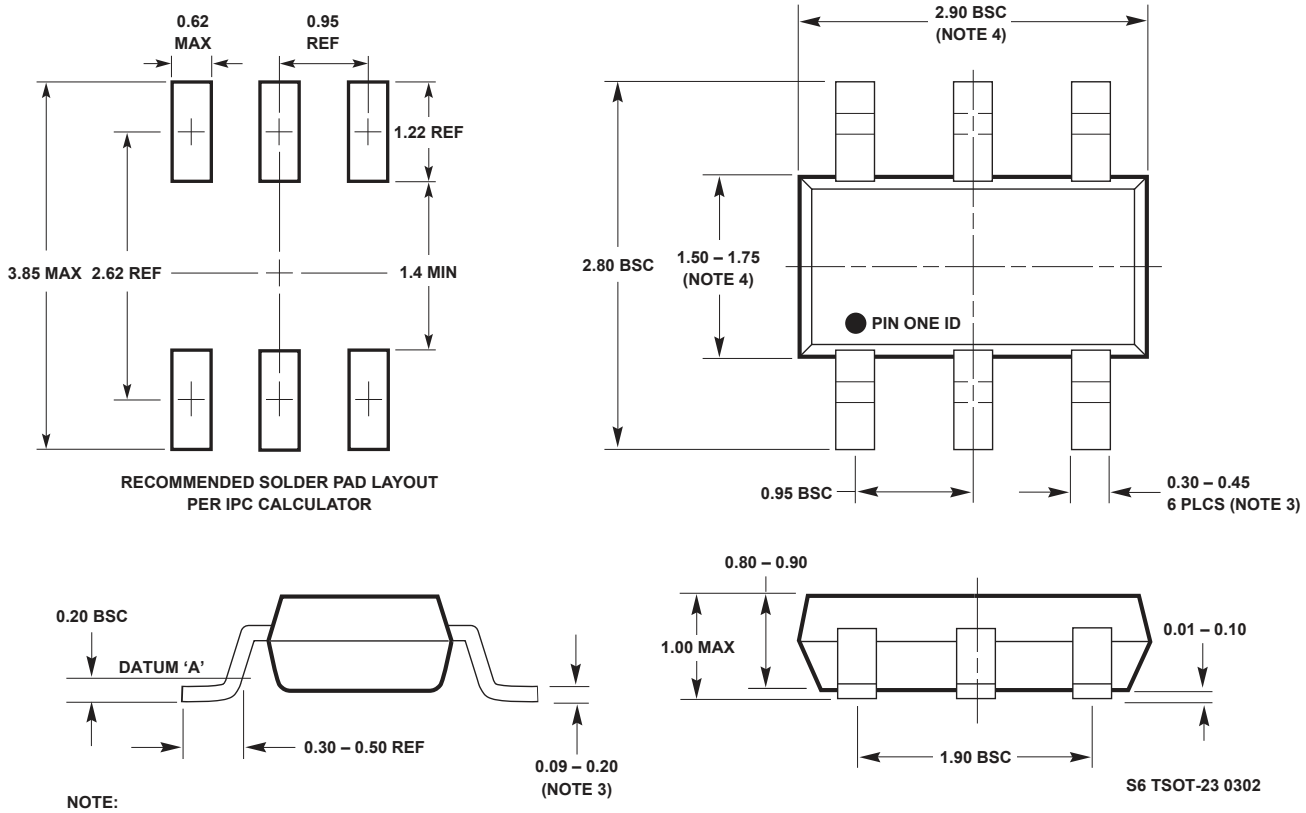
Chip Information (continued)

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

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Ordering Information

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
ADPL21210ECPZ	ADPL21210ECPZ-RL	LY6	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
ADPL21210EUJZ	ADPL21210EUJZ-RL	LY6	6-Lead Plastic TSOT-23	–40°C to 85°C

Consult Analog Devices' Marketing for parts specified with wider operating temperature ranges.

**The temperature grade is identified by a label on the shipping container.*

For more information on lead free part marking, visit Material Declarations.

For more information on tape and reel specifications, visit Tape and Reel Specifications.

Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LT3467A	1.1A (I_{SW}), 2.1MHz, Step-Up DC/DC Converter with Integrated Soft-Start	V_{IN}: 2.4V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 1.2mA, I_{SD} < 1µA, ThinSOT Package.
LT1615/LT1615-1	300mA/80mA (I_{SW}), High Efficiency Step-Up DC/DC Converter	V_{IN}: 1V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LT1618	1.5A (I_{SW}), 1.25MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 1.6V to 18V, $V_{OUT(MAX)}$ = 35V, I_Q = 1.8mA, I_{SD} < 1µA, MS Package
LTC1700	No R_{SENSE}™, 530kHz, Synchronous Step-Up DC/DC Controller	95% Efficiency, V_{IN}: 0.9V to 5V, I_Q = 200µA, I_{SD} < 10µA, MS Package
LTC1871	Wide Input Range, 1MHz, No R_{SENSE} Current Mode Boost, Flyback and SEPIC Controller	92% Efficiency, V_{IN}: 2.5V to 36V, I_Q = 250µA, I_{SD} < 10µA, MS Package
LT1930/LT1930A	1A (I_{SW}), 1.2MHz/2.2MHz, High Efficiency Step-Up DC/DC Converter	High Efficiency, V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1946/LT1946A	1.5A (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter with Soft-Start	High Efficiency, V_{IN}: 2.45V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, MS8 Package
LT1961	1.5A (I_{SW}), 1.25MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 3V to 25V, $V_{OUT(MAX)}$ = 35V, I_Q = 0.9mA, I_{SD} < 6µA, MS8E Package
LTC3400/ LTC3400B	600mA (I_{SW}), 1.2MHz, Synchronous Step-Up DC/DC Converter	92% Efficiency, V_{IN}: 0.85V to 5V, $V_{OUT(MAX)}$ = 5V, I_Q = 19µA/300µA, I_{SD} < 1µA, ThinSOT Package
LTC3401	1A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 38µA, I_{SD} < 1µA, MS Package
LTC3402	2A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 38µA, I_{SD} < 1µA, MS Package
LT3464	85mA (I_{SW}), High Efficiency Step-Up DC/DC Converter with Integrated Schottky and PNP Disconnect	V_{IN}: 2.3V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 25µA, I_{SD} < 1µA, ThinSOT Package

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/26	Initial release	—